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67	US 6267862 B1	45							☑				USPAT
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72	US 6251251 B1	17							☑				USPAT

US-PAT-NO: 6261433

DOCUMENT-IDENTIFIER: US 6261433 B1

TITLE: Electro-chemical deposition system and method of electroplating on substrates

---------- RWIC ----------

Current US Cross Reference Classificatcn - CCXR (12):

205/123

Current US Cross Reference Classification - CCXR (16):

205/157

(12) **United States Patent**
Landau

(10) **Patent No.: US 6,261,433 B1**
(45) **Date of Patent: Jul. 17, 2001**

(54) **ELECTRO-CHEMICAL DEPOSITION SYSTEM AND METHOD OF ELECTROPLATING ON SUBSTRATES**

(75) Inventor: **Uziel Landau**, Cleveland, OH (US)

(73) Assignee: **Applied Materials, Inc.**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/295,678**

(22) Filed: **Apr. 21, 1999**

Related U.S. Application Data

(60) Provisional application No. 60/082,521, filed on Apr. 21, 1998.

(51) Int. Cl.[7] **C25D 5/00**

(52) U.S. Cl. 205/96; 205/103; 205/123; 205/128; 205/149; 205/153; 205/157; 204/297.01; 204/297.03; 204/230.2; 204/230.7; 204/260; 204/261; 204/263; 204/272; 204/273; 204/275.1

(58) Field of Search 204/297.01, 297.03, 204/275.1, 257, 272, 273, 260, 261, 263, 212, 213, 218, 222, 223, 228.9, 229.1, 229.2, 229.6, 230.2, 230.7; 205/96, 103, 123, 126, 149, 153, 157, 291, 292

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3,727,620 4/1973 Orr 134/95

(List continued on next page.)

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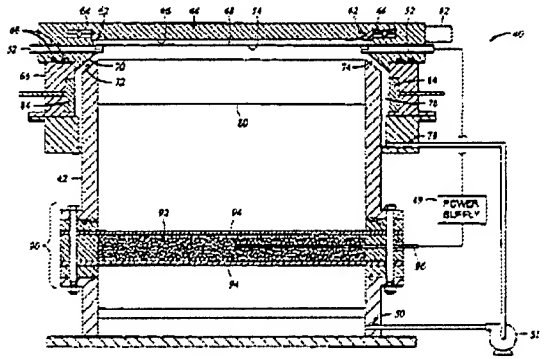
(List continued on next page.)

Primary Examiner—Bruce F. Bell
(74) *Attorney, Agent, or Firm*—Thomason, Moser & Patterson, L.L.P.

(57) **ABSTRACT**

The invention provides an apparatus and a method for achieving reliable, consistent metal electroplating or electrochemical deposition onto semiconductor substrates. More particularly, the invention provides uniform and void-free deposition of metal onto metal seeded semiconductor substrates having sub-micron, high aspect ratio features. The invention provides an electrochemical deposition cell comprising a substrate holder, a cathode electrically contacting a substrate plating surface, an electrolyte container having an electrolyte inlet, an electrolyte outlet and an opening adapted to receive a substrate plating surface and an anode electrically connect to an electrolyte. Preferably, a vibrator is attached to the substrate holder to vibrate the substrate in at least one direction, and an auxiliary electrode is disposed adjacent the electrolyte outlet to provide uniform deposition across the substrate surface. Preferably, a periodic reverse current is applied during the plating period to provide a void-free metal layer within high aspect ratio features on the substrate.

29 Claims, 7 Drawing Sheets



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EAST Browser - 1.1: (516) (205/123)205... | US 6261433 B1 | Tag: S1 Doc: 69/516 (SORTED)

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67	US 6267862 B1	45											USPAT
68	US 6262426 B1	30											USPAT
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70	US 6258240 B1	11											USPAT

US-PAT-NO: 6261433

DOCUMENT-IDENTIFIER: US 6261433 B1

TITLE: Electro-chemical deposition system and method of electroplating on substrates

---------- KWIC ---------

Current US Cross Reference Classification - CCXR (12):

205/123

Current US Cross Reference Classification - CCXR (16):

205/157

4/21/99

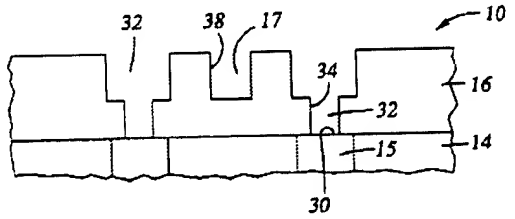

Fig. 1A
(PRIOR ART)

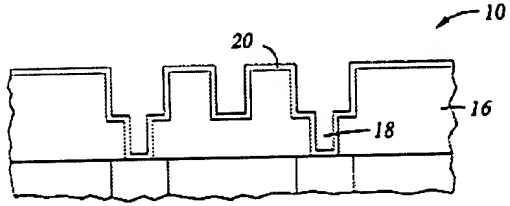

Fig. 1B
(PRIOR ART)

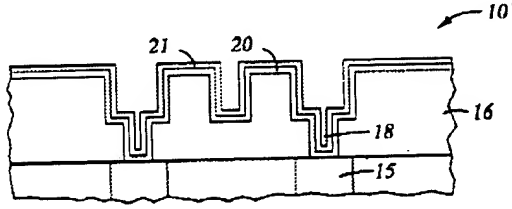

Fig. 1C
(PRIOR ART)

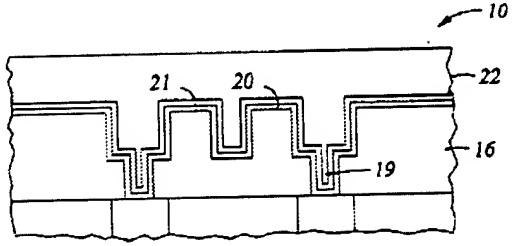

Fig. 1D
(PRIOR ART)

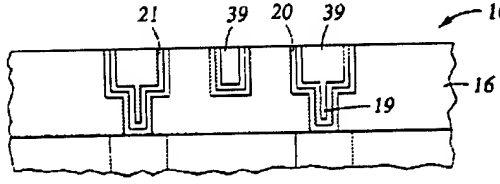

Fig. 1E
(PRIOR ART)

EAST Browser - 1.1: (516) (205/123)205 . [US 6245676 B1 | Tag: S | Doc: 74/516 (SORTED)

File Edit View Tools Window Help

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75	US 6241869 B1	11										USPAT
76	US 6235406 B1	15										USPAT
77	US 6232144 B1	6										USPAT
78	US 6228243 B1	11										USPAT
79	US 6224737 B1	7										USPAT
80	US 6224735 B1	10										USPAT

US-PAT-NO: 6245676

DOCUMENT-IDENTIFIER: US 6245676 B1

TITLE: Method of electroplating copper interconnects

---------- KWIC ----------

Current US Cross Reference Classification - CCXR (3):

205/157

(12) **United States Patent**
Ueno

(10) **Patent No.: US 6,245,676 B1**
(45) **Date of Patent: Jun. 12, 2001**

(54) **METHOD OF ELECTROPLATING COPPER INTERCONNECTS**

(75) Inventor: **Kazuyoshi Ueno**, Tokyo (JP)

(73) Assignee: **NEC Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/255,562**

(22) Filed: **Feb. 22, 1999**

(30) **Foreign Application Priority Data**

Feb. 20, 1998 (JP) 10-038311

(51) **Int. Cl.**[7] **H01L 21/44**; C25D 5/18; C25D 7/12

(52) **U.S. Cl.** **438/687**; 438/677; 438/678; 438/759; 205/103; 205/104; 205/157; 205/220; 205/222

(58) **Field of Search** 438/637–640, 438/643, 408, 676–678, 687, 759; 205/123, 133, 102–104, 157, 107–108, 200, 222

(56) **References Cited**

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57-71150 5/1982 (JP) .

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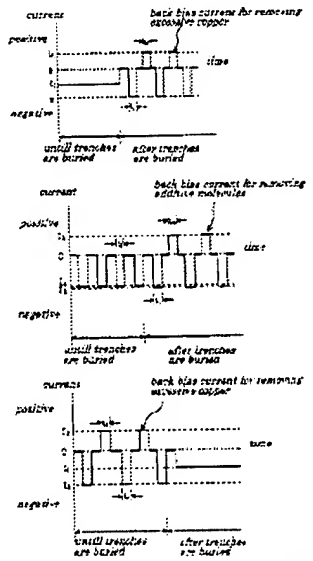
Primary Examiner—Richard Booth
Assistant Examiner—Ha Tran Nguyen
(74) *Attorney, Agent, or Firm*—Hutchins, Wheeler & Dittmar

(57) **ABSTRACT**

The flexibility of a wiring design is improved by preventing any erosion from happening upon forming a buried wiring. An interlayer insulating film is formed on a silicon substrate, and then trenches are formed in the interlayer insulating film. Thereafter, the barrier layer is deposited on side surfaces and a bottom surface in the trenches and on an entire area on the interlayer insulating film, and a copper seed layer is formed over an entire area on the barrier layer. Fountain plating is performed using the copper seed layer as an electrode to deposit the copper plated layer on the trenches and on a peripheral area of the same the copper plated layer buries the trenches and has a protruded configuration. Thereafter, the surface of the copper plated layer is polished with a CMP method until the interlayer insulating film is exposed to form a buried wiring.

9 Claims, 9 Drawing Sheets



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73	US 6251250 B1	17											USPAT
74	US 6245676 B1	20											USPAT
75	US 6241869 B1	11											USPAT

US-PAT-NO: 6245676

DOCUMENT-IDENTIFIER: US 6245676 B1

TITLE: Method of electroplating copper interconnects

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Current US Cross Reference Classification - CCXR (3):

205/157

2/22/94

Fig.2 (a)

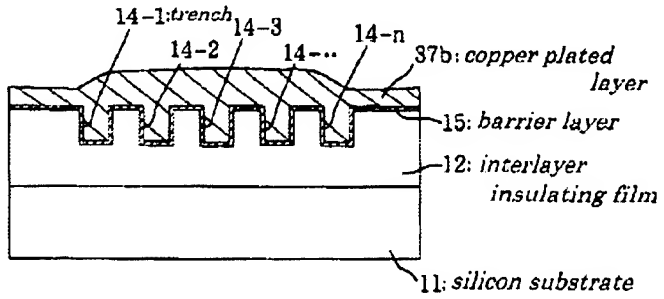


Fig.2 (b)

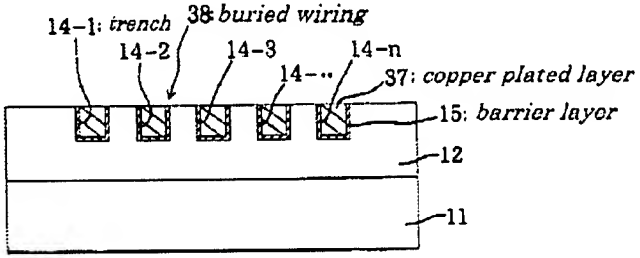
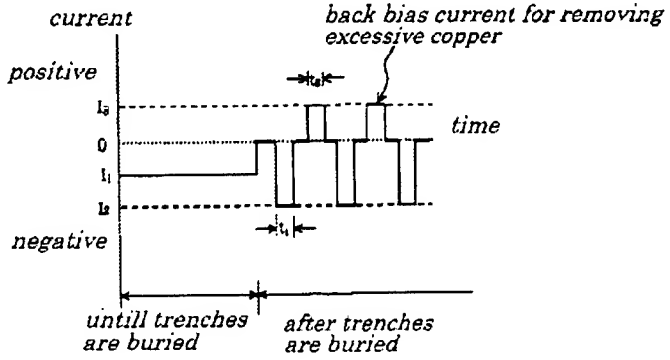


Fig.3



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EAST Browser - L1: (516) (205/123205...) | US 6241869 B1 | Tag: S | Doc: 75/516 (SORTED)

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76	US 6235406 B1	15										USPAT
77	US 6232144 B1	6										USPAT
78	US 6228243 B1	11										USPAT
79	US 6224737 B1	7										USPAT
80	US 6224735 B1	18										USPAT

US-PAT-NO: 6241869

DOCUMENT-IDENTIFIER: US 6241869 B1

TITLE: Apparatus and method for electroplating

---------- KWIC ---------

Current US Cross Reference Classification - CCXR (2):

205/123

Current US Cross Reference Classification - CCXR (3):

205/157

(12) **United States Patent**
Maeda

(10) **Patent No.: US 6,241,869 B1**
(45) **Date of Patent: Jun. 5, 2001**

(54) **APPARATUS AND METHOD FOR ELECTROPLATING**

(75) Inventor: Keiichi Maeda, Kanagawa (JP)

(73) Assignee: Sony Corporation, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/296,297

(22) Filed: Apr. 22, 1999

(30) **Foreign Application Priority Data**

Apr. 24, 1998 (JP) 10-114494

(51) Int. Cl.[7] C25D 5/00; C25D 7/12; C25D 5/34; C25D 5/34; C25D 5/02

(52) U.S. Cl. 205/137; 205/157; 205/159; 205/205; 205/224; 205/118; 205/123

(58) Field of Search 205/157, 159, 205/137, 205, 224, 118, 123; 427/246.1, 294, 383.1

(56) **References Cited**

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5,273,642 * 12/1993 Crites et al. 205/118
5,763,953 * 6/1998 Iijima et al. 257/762

FOREIGN PATENT DOCUMENTS

4-131395 * 5/1992 (JP) .

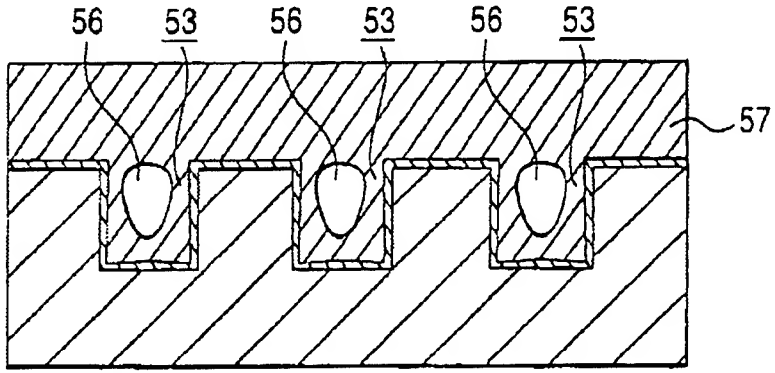
* cited by examiner

Primary Examiner—Edna Wong
(74) *Attorney, Agent, or Firm*—Ronald P. Kananen; Rader, Fishman & Grauer

(57) **ABSTRACT**

An apparatus and a method for electroplating for forming a metal film by an electroplating method. The apparatus comprises a plating bath provided in a non-oxidative atmosphere, and in the method, an article to be plated is immersed in a plating bath through a non-oxidative atmosphere.

7 Claims, 6 Drawing Sheets



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73	US 6251250 B1	17									USPAT
74	US 6245676 B1	20									USPAT
75	US 6241869 B1	11									USPAT
76	US 6235406 B1	15									USPAT

US-PAT-NO: 6241869

DOCUMENT-IDENTIFIER: US 6241969 B1

TITLE: Apparatus and method for electroplating

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Current US Cross Reference Classification - CCXR (2):

205/123

Current US Cross Reference Classification - CCXR (3):

205/157

4/22/99

FIG. 8A

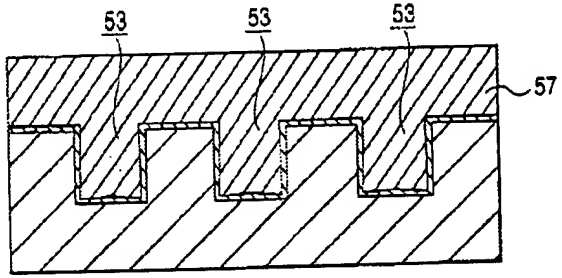
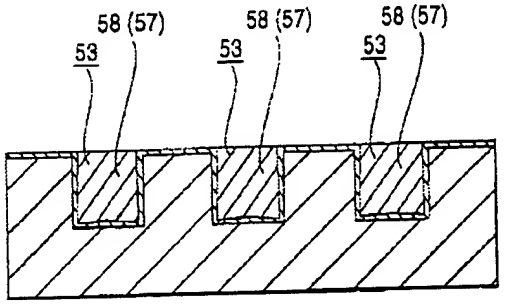


FIG. 8B



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45	US 6331237 B1	7										USPAT
46	US 6319387 B1	17										USPAT
47	US 6319386 B1	7										USPAT
48	US 6319384 B1	12										USPAT
49	US 6315883 B1	18										USPAT

US-PAT-NO: 6319384

DOCUMENT-IDENTIFIER: US 6319384 B1

TITLE: Pulse reverse electrodeposition for metallization and planarization of semiconductor substrates

---------- KWIC ---------

Current US Cross Reference Classification - CCXR (2):

205/123

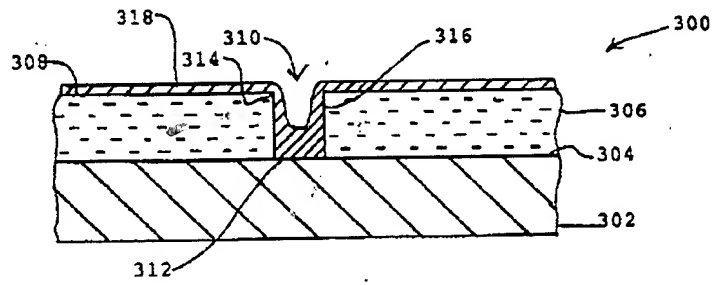

Fig. 3D

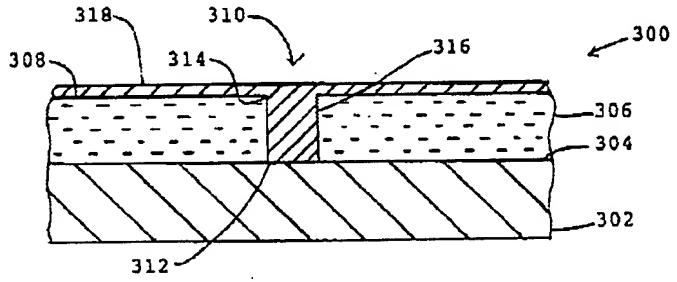

Fig. 3E

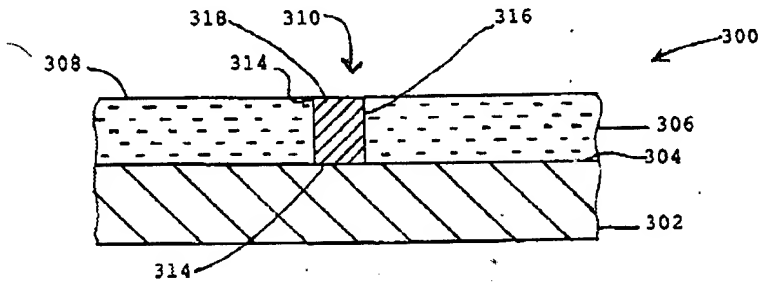

Fig. 3F

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17	US 6448644 B1	13											USPAT
18	US 6444110 B1	7											USPAT
19	US 6440291 B1	10											USPAT
20	US 6440289 B1	9											USPAT
21	US 6436267 B1	22											USPAT

US-PAT-NO: 6440289

DOCUMENT-IDENTIFIER: US 6440289 B1

TITLE: Method for improving seed layer electroplating for semiconductor

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Current US Cross Reference Classification - CCXR (3):

205/123

Current US Cross Reference Classification - CCXR (4):

205/157

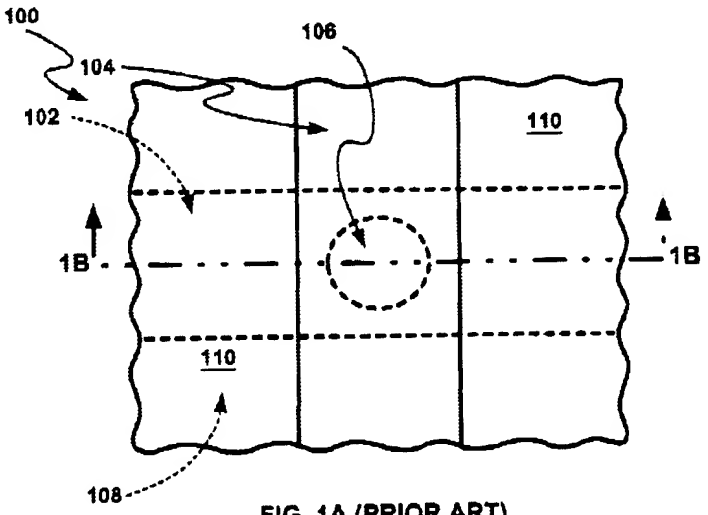

FIG. 1A (PRIOR ART)

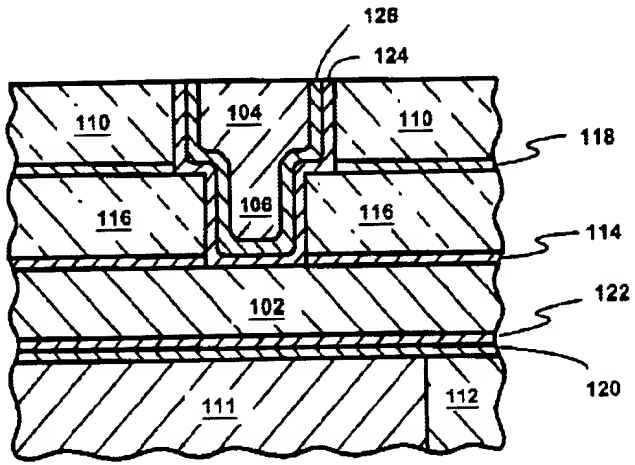

FIG. 1B (PRIOR ART)

EAST Browser - L1: (516) (205/123)205 ... [US 6372114 B1 | Tag: S | Doc: 33/516 (SORTED)]

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32	US 6379522 B1	5											USPAT
33	US 6372114 B1	14											USPAT
34	US 6370768 B1	23											USPAT
35	US 6361675 B1	10											USPAT
36	US 6358388 B1	59											USPAT
37	US 6350364 B1	6											USPAT

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US-PAT-NO: 6372114

DOCUMENT-IDENTIFIER:  US 6372114 B1

TITLE:  Method of forming a semiconductor device

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Current US Cross Reference Classification - CCXR (2):

205/123
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(12) **United States Patent**
Ito

(10) **Patent No.: US 6,372,114 B1**
(45) **Date of Patent: Apr. 16, 2002**

(54) **METHOD OF FORMING A SEMICONDUCTOR DEVICE**

(75) Inventor: **Nobukazu Ito**, Tokyo (JP)

(73) Assignee: **NEC Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/288,265**

(22) Filed: **Apr. 8, 1999**

(30) **Foreign Application Priority Data**

Apr. 8, 1998 (JP) 10-095502

(51) **Int. Cl.**[7] **C25D 5/02**; C23C 14/34; H01L 21/44

(52) **U.S. Cl.** 205/118; 205/123; 204/192.17; 438/653; 438/656; 438/666; 438/672; 438/674; 438/675; 438/685; 438/687

(58) **Field of Search** 204/192.15, 192.17; 438/652, 653, 656, 666, 669, 672, 674, 675, 685, 687; 205/118, 123; 427/97, 98, 250, 259, 282

(56) **References Cited**

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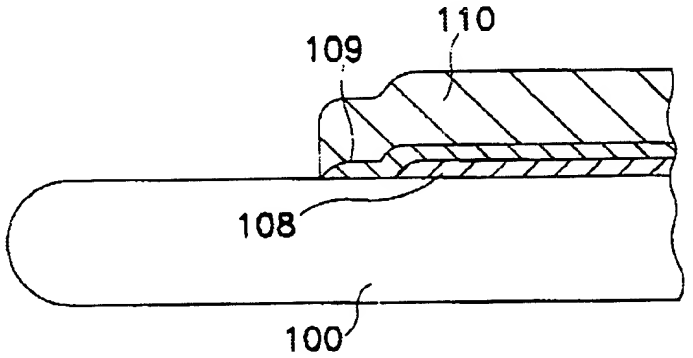
Primary Examiner—Rodney G. McDonald
(74) *Attorney, Agent, or Firm*—Hayes, Soloway, Hennessey, Grossman & Hage, P.C.

(57) **ABSTRACT**

A method of forming a multi-layer structure over an insulating layer comprises the steps of: selectively depositing a barrier layer on a predetermined region of an insulating layer by use of a first deposition mask; selectively depositing a metal seed layer made of a metal which is different in substance from the barrier layer by use of a second deposition mask, so that the metal seed layer extends not only on an entire surface of the barrier layer but also a peripheral region positioned outside the predetermined region of the insulating layer; and forming a metal plating layer made of the metal of the metal seed layer, so that the metal plating layer is adhered on the metal seed layer whereby the metal plating layer is separated from the barrier layer and also from the insulating layer.

6 Claims, 7 Drawing Sheets



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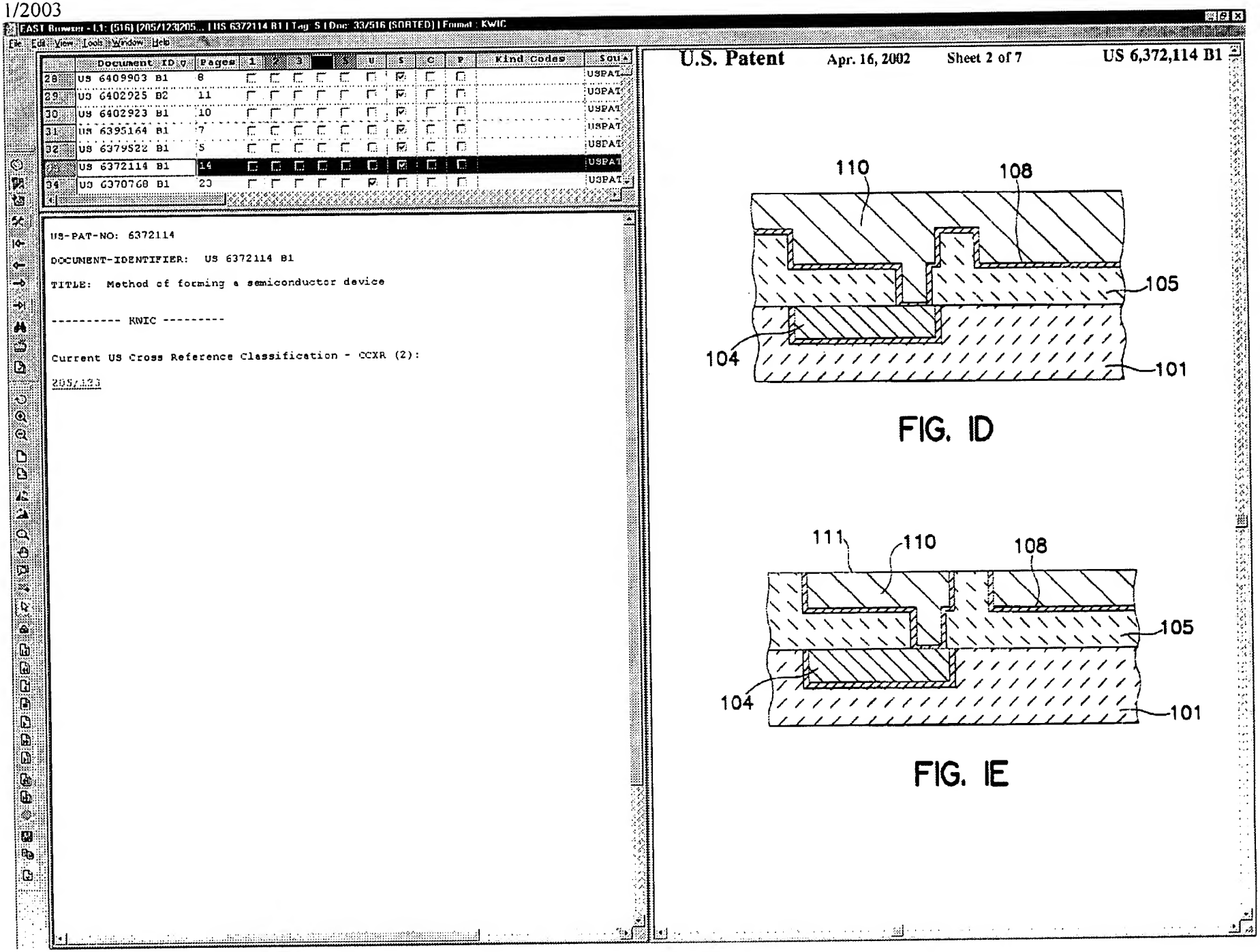

FIG. ID

FIG. IE

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33	US 6372114 B1	14										USPAT
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36	US 6358388 B1	59										USPAT
37	US 6350364 B1	6										USPAT
38	US 6350363 B1	10										USPAT

US-PAT-NO: 6350364

DOCUMENT-IDENTIFIER: US 6350364 B1

TITLE: Method for improvement of planarity of electroplated copper

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Current US Cross Reference Classification - CCXR (1):

205/157

(12) **United States Patent**
Jang

(10) **Patent No.: US 6,350,364 B1**
(45) **Date of Patent: Feb. 26, 2002**

(54) METHOD FOR IMPROVEMENT OF PLANARITY OF ELECTROPLATED COPPER

(75) Inventor: Syun-Ming Jang, Hsin-Chu (TW)

(73) Assignee: Taiwan Semiconductor Manufacturing Company, Hsin-Chu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/506,931

(22) Filed: Feb. 18, 2000

(51) Int. Cl.[7] C25D 5/02; C25D 7/12; C25D 5/10

(52) U.S. Cl. 205/118; 205/157; 205/170; 205/182

(58) Field of Search 205/118, 157, 205/170, 182

(56) **References Cited**

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6,168,794	B1 *	5/2001	Brown et al.	205/116
B16,224,737	*	5/2001	Tsai et al.	205/123

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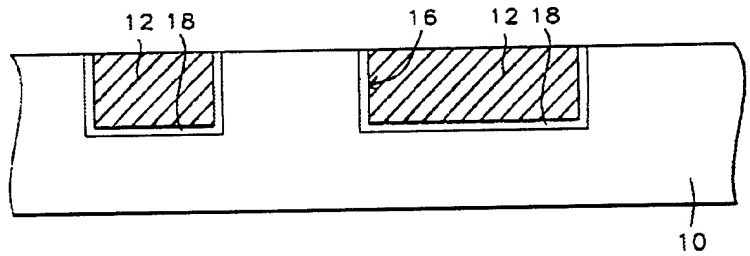
Primary Examiner—Kathryn Gorgos
Assistant Examiner—Erica Smith-Hicks
(74) *Attorney, Agent, or Firm*—George O. Saile; Stephen B. Ackerman; Stephen G. Stanton

(57) **ABSTRACT**

A method for electroplating copper in trenches, including the steps of providing a semiconductor substrate having a trench formed therein and electrolytically depositing a first copper containing layer having an upper surface and a predetermined thickness within the trench. The first copper deposition step has a first ratio of brighteners concentration: levelers concentration. Then a second copper containing layer having an upper surface and a predetermined thickness is electrolytically deposited over the first copper containing layer. The second copper deposition step has a second ratio of brighteners concentration:levelers concentration that is less than the said first ratio of brighteners concentration:levelers concentration. The second copper containing layer upper surface having a greater planarity than the first copper containing layer upper surface due to an increased concentration of levelers relative to the brighteners in the electrolytic bath.

20 Claims, 1 Drawing Sheet



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EAST Browser - L1: (516) (205/123)205... | US 6315883 B1 | Tag: S | Doc: 49/516 (SORTED)

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	Document ID	Pages	Kind Codes	Source
49	US 6315883 B1	18		USPAT
50	US 6309782 B1	21		USPAT
51	US 6309528 B1	12		USPAT
52	US 6303014 B1	24		USPAT
53	US 6300244 B1	19		USPAT
54	US 6299753 B1	14		USPAT
55	US 6299751 B1	45		USPAT

US-PAT-NO: 6315883

DOCUMENT-IDENTIFIER: US 6315883 B1

TITLE: Electroplanarization of large and small damascene features using diffusion barriers and electropolishing

---------- KWIC ---------

Current US Original Classification - CCOR (1):

205/123

Current US Cross Reference Classification - CCXR (1):

205/157

(12) **United States Patent**
Mayer et al.

(10) **Patent No.: US 6,315,883 B1**
(45) **Date of Patent: Nov. 13, 2001**

(54) **ELECTROPLANARIZATION OF LARGE AND SMALL DAMASCENE FEATURES USING DIFFUSION BARRIERS AND ELECTROPOLISHING**

(75) Inventors: **Steven T. Mayer**; **Robert J. Contolini**, both of Lake Oswego, OR (US)

(73) Assignee: **Novellus Systems, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/412,837

(22) Filed: **Oct. 5, 1999**

Related U.S. Application Data

(60) Provisional application No. 60/105,700, filed on Oct. 26, 1998

(51) Int. Cl.[7] C25D 5/02; C25D 5/48; C25D 7/12; C25F 3/16

(52) U.S. Cl. 205/123; 205/220; 205/157; 205/640

(58) Field of Search 205/640, 123, 205/157, 220

(56) **References Cited**

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Robert J. Contolini, Anthony P. Bernhard, and Steven T. Mayer, Electrochemical Planarization for Multilevel Metallization, J. Electrochem Soc., vol. 141, No. 9, Sep. 1994, 9 pages.

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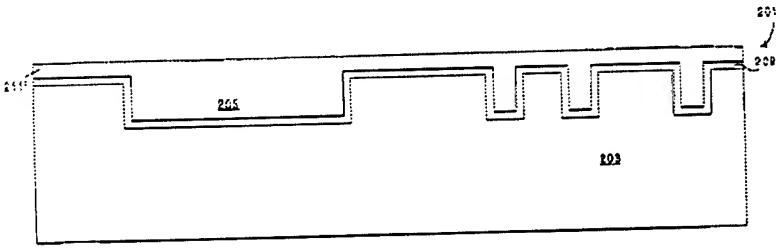
Primary Examiner—Donald R. Valentine
(74) *Attorney, Agent, or Firm*—Beyer Weaver & Thomas LLP

(57) **ABSTRACT**

A disclosed electroplanarization process involves "masking" certain regions of a wafer surface during electropolishing. The regions chosen for masking are features of relatively low aspect ratio (i.e., features that are wider than they are deep). The masking is accomplished with a material of relatively low ionic conductivity, which effectively slows or blocks transport of the metal ions produced during electropolishing. Examples of masking materials include concentrated phosphoric acid and certain polymers.

32 Claims, 9 Drawing Sheets



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45	US 6331237 B1	7											USPAT
46	US 6319387 B1	17											USPAT
47	US 6319386 B1	7											USPAT
48	US 6319384 B1	12											USPAT
49	US 6315883 B1	18											USPAT
50	US 6309782 D1	21											USPAT

US-PAT-NO: 6315883

DOCUMENT-IDENTIFIER: US 6315883 B1

TITLE: Electroplanarization of large and small damascene features using diffusion barriers and electropolishing

---------- KWIC ---------

Current US Original Classification - CCOR (1):

205/123

Current US Cross Reference Classification - CCXR (1):

205/157

10/5/99

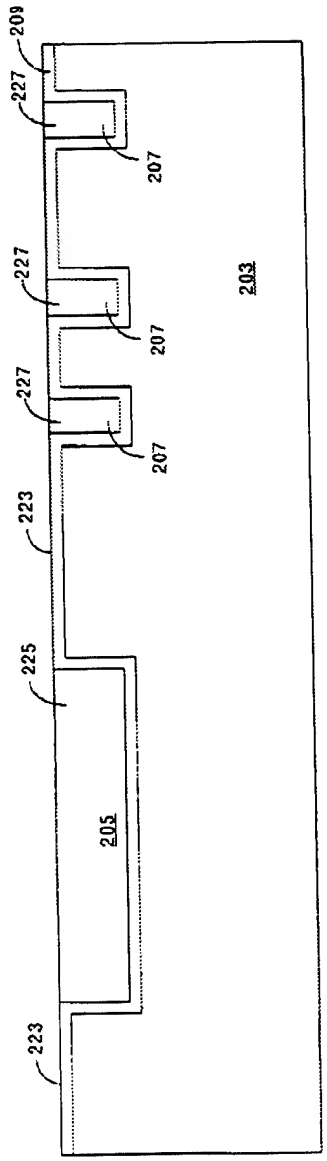

FIG. 8

FAST Browser - L1: (516) (205/123)205... | US 6300244 B1 | Tag: S | Doc: 53/516 (SORTED)

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	Document ID	Pages	1	2	3	T	U	S	C	P	Kind Codes	Sou
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54	US 6299753 B1	14						☑				USPAT
55	US 6299751 B1	45						☑				USPAT
56	US 6297157 B1	9						☑				USPAT
57	US 6296753 B1	45						☑				USPAT
58	US 6287493 B1	45						☑				USPAT
59	US 6204121 B1	8						☑				USPAT

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US-PAT-NO: 6300244

DOCUMENT-IDENTIFIER:  US 6300244 B1

TITLE:  Semiconductor device and method of manufacturing the same


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Current US Cross Reference Classification - CCXR (3):

205/123
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(12) **United States Patent**
Itabashi et al.

(10) **Patent No.: US 6,300,244 B1**
(45) **Date of Patent: Oct. 9, 2001**

(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

(75) Inventors: **Takeyuki Itabashi; Toshio Haba; Haruo Akahoshi**, all of Hitachi (JP)

(73) Assignee: **Hitachi, Ltd.**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/317,955**

(22) Filed: **May 25, 1999**

(30) **Foreign Application Priority Data**

May 25, 1998 (JP) 10-143133

(51) Int. Cl.[7] H01L 21/24; H01L 21/4763; B01D 57/02; C25D 5/02; B05D 5/12

(52) U.S. Cl. 438/678; 438/622; 438/629; 438/688; 438/687; 204/450; 204/489; 205/123; 205/125; 427/98

(53) Field of Search 438/678, 403, 438/688, 687, 675, 622, 625, 627, 629; 427/97, 98, 443.1, 437, 304, 305; 204/471, 489, 492, 496, 499, 450; 205/123, 125, 126

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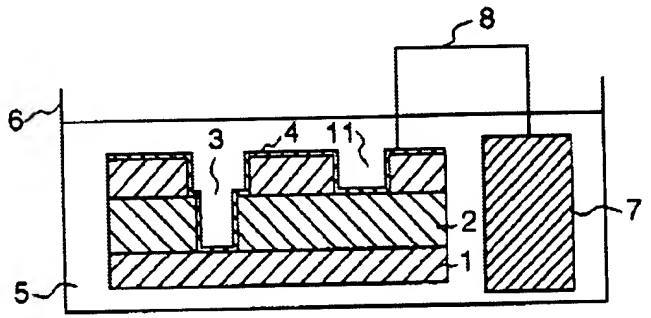
Primary Examiner—Charles Bowers
Assistant Examiner—Thanhha Pham
(74) *Attorney, Agent, or Firm*—Antonelli, Terry, Stout & Kraus, LLP

(57) **ABSTRACT**

When a wiring conductor is formed on a semiconductor substrate, a via-hole or a trench is formed by directly performing electroless plating on a barrier layer containing a very small depressed portion such as the via-hole or the trench in an insulator layer without using a dry metallized method or a substitutive plating method.

The semiconductor device is provided with an insulator layer having a via-stud on a semiconductor substrate, the via-stud being formed in a via-hole through a barrier layer formed of an inorganic compound layer or a high melting point metal layer formed on an inner surface of the via-hole, the via-stud being made of the same metal as a metal composing the barrier layer. The semiconductor device can be obtained by forming the barrier layer on the inner surface of the via-hole in the semiconductor substrate, then treating the substrate with a treatment solution containing a complex forming agent, immersing the treated substrate into an electroless plating solution, bringing a member made of the same metal as a metal formed by the electroless plating in contact with the electroless plating solution, and electrically connecting the member to the barrier layer to perform electroless plating.

18 Claims, 8 Drawing Sheets



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48	US 6319384 B1	12										USPAT
49	US 6315883 B1	18										USPAT
50	US 6309782 B1	21										USPAT
51	US 6309528 B1	12										USPAT
52	US 6303014 B1	24										USPAT
53	US 6300244 B1	19										USPAT
54	US 6299753 B1	14										USPAT

US-PAT-NO: 6300244

DOCUMENT-IDENTIFIER: US 6300244 B1

TITLE: Semiconductor device and method of manufacturing the same

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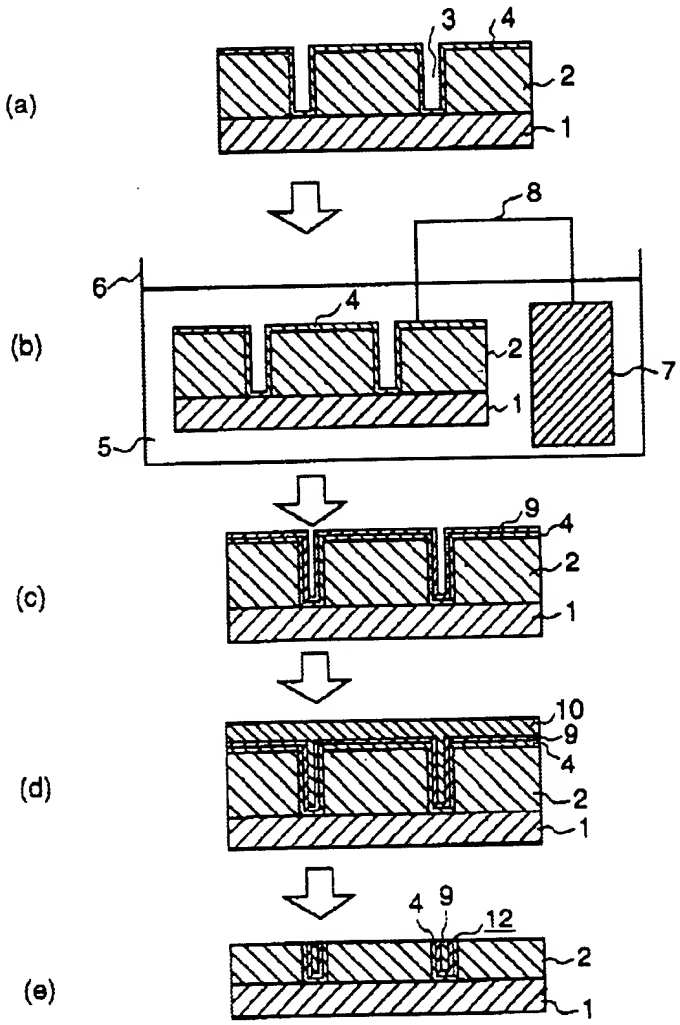
Current US Cross Reference Classification - CCXR (3):

205/123

5/25/99

FIG.1



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55	US 6299751 B1	45										USPAT
56	US 6297157 B1	9										USPAT
57	US 6296753 B1	45										USPAT
58	US 6287443 B1	45										USPAT
59	US 6284121 B1	8										USPAT
60	US 6277262 B1	10										USPAT
61	US 6277260 B1	45										USPAT

US-PAT-NO: 6297157

DOCUMENT-IDENTIFIER: US 6297157 B1

TITLE: Time ramped method for plating of high aspect ratio semiconductor vias and channels

---------- KWIC ---------

Current US Cross Reference Classification - CCXR (2):

205/123

(12) **United States Patent**
Lopatin et al.

(10) **Patent No.: US 6,297,157 B1**
(45) **Date of Patent: Oct. 2, 2001**

(54) **TIME RAMPED METHOD FOR PLATING OF HIGH ASPECT RATIO SEMICONDUCTOR VIAS AND CHANNELS**

(75) Inventors: **Sergey D. Lopatin**, Santa Clara; **Matthew S. Buynoski**, Palo Alto, both of CA (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/431,516

(22) Filed: Nov. 1, 1999

(51) Int. Cl.[7] H01L 21/44; H01L 21/4763; C15D 5/18; C25D 5/02

(52) U.S. Cl. 438/687; 438/622; 438/625; 438/638; 438/672; 438/675; 438/686; 205/102; 205/123

(58) Field of Search 438/687, 678, 438/622, 625, 637, 638, 686, 672, 674, 675; 205/102, 103, 104, 123

(56) **References Cited**

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Yosi Shacham-Diamand & Sergey Lopatin, "High Aspect Ratio Quarter-Micron Electroless Copper Integrated Technology", *Microelectronic Engineering*, 37/38, 1997, pp. 77–78.

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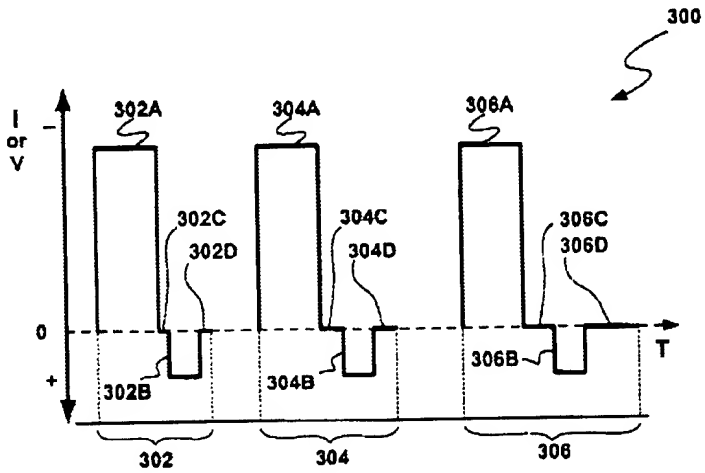
Primary Examiner—Charles Bowers
Assistant Examiner—Thanhha Pham
(74) *Attorney, Agent, or Firm*—Mikio Ishimaru

(57) **ABSTRACT**

A method is provided for forming conductive layers in semiconductor vias by using forward and reverse pulses during the electroplating process which have time intervals between pulses which increase with time and for forming conductive layers in semiconductor channels by using forward pulses during the electroplating process which have time intervals between pulses which also increase with time. This allows fast deposition while reducing the deposition stress to eliminate voids and speeds up the overall manufacturing process.

20 Claims, 3 Drawing Sheets



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54	US 6299753 B1	14													USPAT
55	US 6299751 B1	45													USPAT
56	US 6297157 B1	9													USPAT
57	US 6296753 B1	45													USPAT

US-PAT-NO: 6297157

DOCUMENT-IDENTIFIER: US 6297157 B1

TITLE: Time ramped method for plating of high aspect ratio semiconductor vias and channels

---------- KWIC ----------

Current US Cross Reference Classification - CCXR (2):

205/123

11/1/99

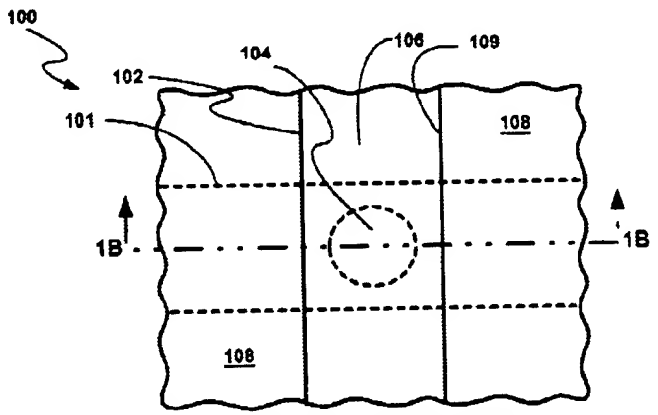

FIG. 1A (PRIOR ART)

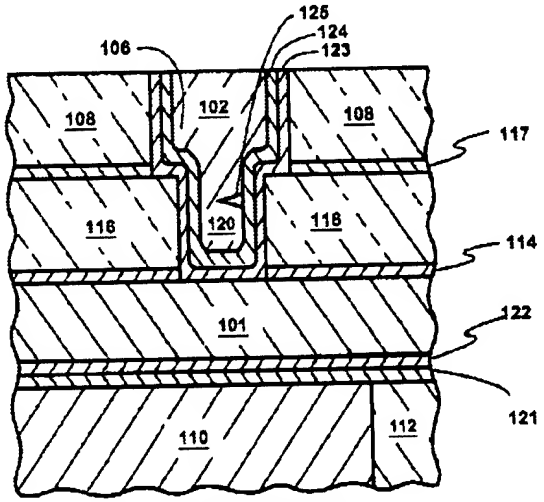

FIG. 1B (PRIOR ART)